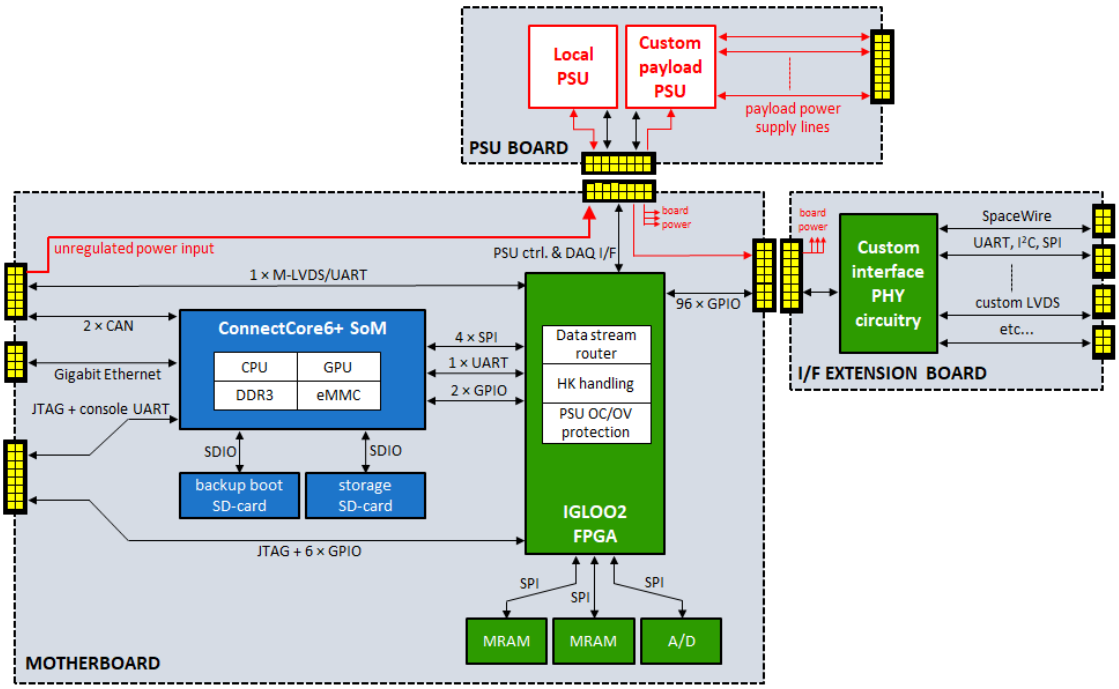
CHP – OBC

Customizable High Performance On-Board Computer

The CHP-OBC is a general-purpose computation platform for nano- and microsatellites. It provides high computation capacity, versatile and flexible interface capabilities, and robust and reliable power supply for payload subsystems.

Main features:

- High computational & storage capacity
- Full-featured Linux environment for application development
- Highly customizable interface set
- Wireless link for development-time debug purposes



Further technical information	
Central microprocessor	Quad-core Cortex-A9
µP core frequency	Up to 850 MHz
RAM	2 GB DDR3
Mass storage	5 GB on-chip eMMC, removable SD-card, up to 128 GB
Operating system	Yocto Linux[1]
Interfaces	Gigabit Ethernet 2 × CAN 2 × M-LVDS/UART console UART WiFi Optional interfaces[2]: 96 × GPIOs for the followings: • UART / SPI / I^2C • SpaceWire (ECSS-E-ST-50-12C) • LVDS lines with custom data link protocols
Application development support	• Board Support Package written in C/C++ provided by C3S • Python with open-source packages (e.g. NumPy, SciPy, Pandas, etc.) • Other standard programming and scripting languages and application-specific packages
Power supply	9.9 V – 16.8 V
Dimensions	≈ 95 × 90 × 35 mm
Mass	≈ 200 g
Operation temperature range	-40 … +85 °C

[1] C implementation of HAL API is provided
[2] FPA-based interface circuitry + additional extension board. The maximal number of different interface types may depend on the specific interface configuration.

Central processor & storage:

The central processor system of the CHP-OBC is a highly integrated SoM (System-on-Module) provided by DIGI International. The ConnectCore6+ SoM integrates a **quad-core Cortex-A9**-based SoC (System-on-Chip), **2 GB DDR3 RAM**, **8 GB on-chip eMMC** with customizable partitioning structure and up to **5 GB user data** storage capacity. The SoC of the module includes hardware **graphics accelerators** and an **image processing unit**. The module has an SDIO interface and an external **SD-card slot** making the storage media easily removable during the software development phase.

Interface extensions:

The interface capabilities of the ConnectCore6+ SoM are extended by a Microchip IGLOO2 FPGA device (M2GL090-FGG484I) with a pre-defined internal logic design with the following features[3]:

- Run-time configurable **routing capabilities** between the SoM and the external payload subsystems
  - 4 × SPI-based data stream interfaces towards the SoM
  - 1 × UART interface for routing and remote payload subsystem configuration / HK
  - SoM data stream interfaces forwarded to **up to 15 remote payload subsystems** with application-specific data-link layer protocols (e.g. SpaceWire, custom-LVDS, etc.)
  - **Run-time configurable routing** (time-division multiplexing / parallelism) among data stream interfaces for shared-payload bandwidth optimization
- On-board housekeeping telemetry gathering with external 12-bit A/D-converters
- Configurable control and **OC/OV protection** circuitry for the payload power supply submodule

[3] HAL API for the interface extension services is provided by C3S

Payload power supply provision:

The CHP-OBC provides the payload subsystems with run-time controllable, protected secondary power supply lines with the following characteristics:

- Flexible architecture: up to 10 LCLs
- Robustness
  - **Single-point failure tolerant LCLs**
  - **SEL (Single-Event Latch-up) tested design**
- Configurability: class 1-4 (1 A … 4 A) LCLs
- Output voltage: 9.9 V … 16.8 V
- Peak power per LCL: **up to 50 W**
- Total output peak power for the whole payload-bay[4]: 165 W
- Full telemetry service: output current / voltage measurement per LCL

Application use cases:

The versatile architecture of the CHP-OBC makes it suitable for different application areas, such as **avionics** control, traditional or AI/ML-based **on-board autonomous spacecraft operation**, pre-processing for **link budget optimization**, etc. Use it as a…

- **payload controller** being part of C3S' CubeSat platform or other spacecraft platforms:
  - interface extension logic adaptation to mission-specific payload subsystems' needs is done by C3S.
  - Use its central processor as a computation platform for **software IOD** purposes. Run-time environment provided by C3S.
  - Use its on-board FPGA as a programmable logic platform for **VHDL IP core IOD** purposes. Customer IP core integration is done by C3S.
- **customizable on-board computer**
  - Only-HW way: SoM with Linux is provided by C3S. "Empty" FPGA is provided, it **can be programmed by the customer** using standard JTAG interface and programmer solutions provided by the FPGA vendor (Microchip).
  - Full-featured way: **SoM with Linux +** standard / customer-defined **interface extension logic** for the FPGA (together with HAL API) is provided by C3S.

[4] Can be exceeded for a short period of time (<< 1 sec)