Completed as a **multi-output low-noise SMPS** for the SMILE satellite **in cooperation with ESA**, this PSU BreadBoad design was accepted by the agency TRL 4.

Breadboard design was implemented using COTS components with Space-grade substitutes and outlines in mind, so that the same card size can be achieved in the FM.

Both converters are implemented using a galvanically isolated Forward-architecture with common CM+DM Filters on the input.

The SMPS' have operating frequencies of:

- 250 kHz (synchronized)
- 220 kHz (free-running)

The PSU also features synchronized magnetic feedback with a synchronized frequency of 5 MHz and a free-running frequency of 4.3 MHz.

Compliance with standards:

- Derating: ***ECSS-Q-ST-30-11C***
- CE of CM and DM Noise, Inrush current: ***ECSS-E-ST-20-07C*** *(Sub-system and equipment limits)*

Input protections

- Under-voltage Lockout
- Optional input LCL (Overcurrent protection)

Optional output features

- Overcurrent and overvoltage protection
- Off-the-shelf and custom LDO
- DM and CM filter

Design versions:

The simplest design features no HK data collection, and only basic overcurrent protection for the outputs.

Optional HK data:

- Overcurrent and overvoltage signals from output channels
- Input UVLO signal
- "Voltage good" signals (window compara-tors on all outputs)
- Temperature (AD590MF sensor)

These data and the circuit protection can be handled with either:

- A HK&DAQ block made of discrete digital components - Data decoding and provi-sion to a unique digital bus
- An FPGA HK&DAQ block - Complete digi-tal interface (implementing the slave side of the C3S RoR communication protocol), customizable overcurrent-overvoltage timings, etc. Additional digital functions can be implemented according to user needs.

FM radiation level: TID: 50 krad

Temperature range: [-40°C, +60°C]

Figure 1: EBB of the customizable PSU

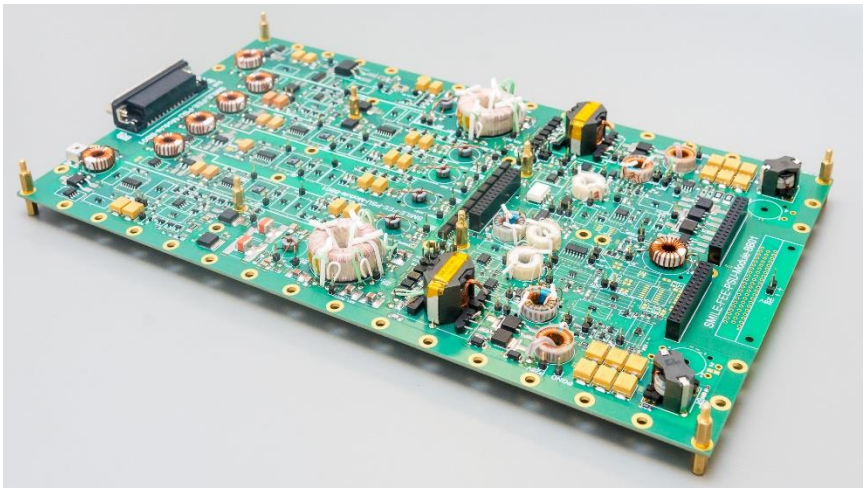

Table 1: FPGA HK&DAQ block parameters

Target device family	Parameters (can be varied according to user needs)	Seq	Comb
RTSX / RTAX	global clock frequency: 10 MHz UART baudrate: 200 kbps	490	1100
ProASIC3E		460	1340

Table 2: Output parametes

	Implemented parameters		Customizable parameters		
Channel	**Nominal voltage**	**Maximum current**	**Minimum voltage**	**Maximum voltage**	**Maximum current**
PSU_A_1	31.65 V	87 mA	3.3 V	35 V	2 A
PSU_A_2	6.45 V	144 mA	3.3 V	35 V	2 A
PSU_A_3	6.45 V	44 mA	3.3 V	35 V	2 A
PSU_A_4	-6.45 V	-170 mA	3.3 V	35 V	2 A
PSU_B_1	15.85	172 mA	3.3 V	35 V	2 A
PSU_B_2	4.45	420 mA	3.3 V	35 V	2 A
PSU_B_3	-	-	3.3 V	35 V	2 A

Note: 35 V is only viable on one output/converter. Please contact us with your preliminary channel voltage plan for more information.

Maximum possible output power on the two converters combined is 60 W.

Table 3: Input parameters

Implemented minimum voltage	Implemented nominal voltage	Implemented maximum voltage	Customizable minimum voltage	Customizable maximum voltage
23.5 V	28 V	32.5 V	10V	400V

Note 1: The narrower the input voltage range, the more efficient the converter can be. The maximal factor of input voltage range (max voltage/min voltage) is that is doable is ~2 with the forward architecture.

Note 2: There are sharp rises in mass and volume where there needs to be a switch between capacitor voltage ratings (60V, 120V, 300V, as ECSS deratings must apply).

Figure 2: Block diagram of the customizable PSU