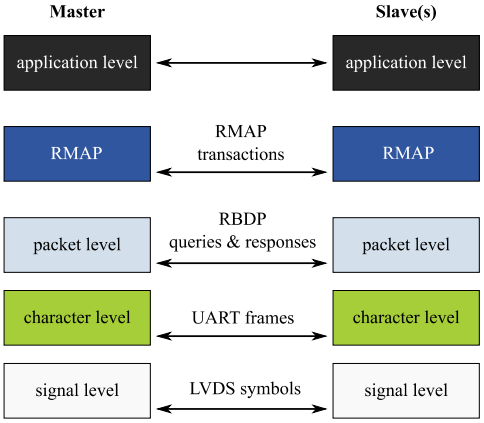
RoR communication protocol stack

RoR is a general-purpose, lightweight serial communication protocol stack for **housekeeping data acquisition and control** of remote submodules. The lower 3 layers of the stack are together called Regular Bytestream DAQ Protocol (RBDP) and the upper layer augmenting it is called Remote Memory Access Protocol (RMAP). The 4 layers together compose the complete RMAP over RBDP (RoR) protocol stack.



The protocol stack can be used in a **point-to-point** connection topology with a single master and a single slave or in a single-master/multi-slave, **M-LVDS**-based connection scheme with up to 256 RBDP or 32 RMAP slave entities.

The character level of the protocol stack uses 9O1 UART frames as the basic unit of information, and performs bit error checks (start bit, stop bit, parity). The UART signaling rate is not limited by the protocol, it can be fitted to the application needs.

The packet level defines higher level information units as coherent sets of characters. Two types of packets are defined: single-character query packets sent by the master and multi-character (up to 16) response packets sent by the slave(s). The packet level provides optional **CRC check**. Packet level defines bus access timing characteristics and implements a **simple bus arbitration** scheme. Additionally, packet level also defines query and response error handling mechanisms and implements basic **bus contention error mitigation**. Several high-level use-cases are recommended by the RBDP protocol definition:

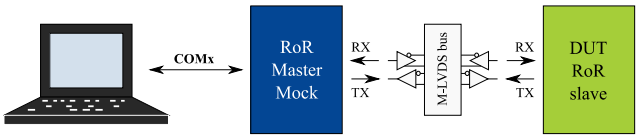
- Periodically refreshed memory map
- Range addressing for structured or hierarchical slave nodes
- Overlapping slave address ranges – posted broadcast messaging
- Commanding through RBDP

RMAP is an additional layer over RBDP packet level implementing simple **memory read and memory write services**. Using this abstraction, all slave entities can be considered unique memory maps (up to 512×8-bit entries) from the master's point-of-view. This makes master/slave interface documentation easy, consistent, and straightforward.

VHDL IP cores

A comprehensive set of VHDL IP cores is available to make rapid prototyping of RoR-based architectures possible using programmable logic devices:

- **RBDP master/slave IP cores** implement character and packet level services.
- **RMAP master/slave IP cores** implement read and write services.
- **RoR Master Mock IP core**: Intended to be used for prototype validation of any design entities implementing the slave side of the RoR protocol stack. Python-based API and GUI are available.



The VHDL models of the IP cores…

- are completely **technology-independent**, and are tested in Microsemi, Intel, and Xilinx devices.
- do not require block-RAM modules.
- are constructed in a **HiRel design approach** including fail-safe FSMs capable of automatically recover from invalid states caused by SEUs. Higher level error information gathering is supported by generating error signals on the host interfaces. HiRel capabilities do not rely on the target technology.

RBDP master IP core

Target	Parameters	Seq	Comb
XC3S500E	global clock frequency: 50 MHz reply packet data bytes: 5 CRC: yes UART baudrate: 200 kbps	320	650 (4-LUTs)
EP3C16		320	680 (4-LUTs)
A3PE1500		320	850 (3-LUTs)

RBDP slave IP core

Target	Parameters	Seq	Comb
XC3S500E	global clock frequency: 50 MHz reply packet data bytes: 5 CRC: yes UART baudrate: 200 kbps	320	670 (4-LUTs)
EP3C16		320	700 (4-LUTs)
A3PE1500		320	910 (3-LUTs)

RoR (RBDP+RMAP) **master IP core**

Target	Parameters	Seq	Comb
XC3S500E	global clock frequency: 50 MHz UART baudrate: 200 kbps	370	780 (4-LUTs)
EP3C16		380	780 (4-LUTs)
A3PE1500		380	1050 (3-LUTs)

RoR (RBDP+RMAP) **slave IP core**

Target	Parameters	Seq	Comb
XC3S500E	global clock frequency: 50 MHz UART baudrate: 200 kbps	330	840 (4-LUTs)
EP3C16		350	770 (4-LUTs)
A3PE1500		340	1040 (3-LUTs)

RoR Master Mock IP core

Target	Parameters	Seq	Comb
XC3S500E	global clock frequency: 50 MHz UART baudrate (PC): 115.2 kbps UART baudrate (RoR): 9.6 kbps	700	1500 (4-LUTs)
EP3C16		700	1400 (4-LUTs)
A3PE1500		700	1600 (3-LUTs)