Completed as a **multi-output low-noise SMPS** for the SMILE satellite **in cooperation with ESA**, this PSU BreadBoad and currently is at CDR level (TRL 5).

The design was completed according to specifications received from Syderal Swiss to an existing space sector need.

Breadboard design was implemented using COTS components with Space-grade substitutes and outlines in mind, so that the same card size can be achieved in the FM.

The SMPS was implemented with a forward architecture, using operating frequencies of:

- 180-220 kHz (synchronized)
- 165kHz (free-running)

The PSU also features a **magnetic feedback** with a free-running frequency of 2 MHz.

Compliance with standards:

- Derating: ***ECSS-Q-ST-30-11C***
- CE of CM and DM Noise, Inrush current: ***ECSS-E-ST-20-07C*** *(Sub-system and equipment limits)*
- TMTC interfaces: **ECSS-E-ST-50-14C**

Output channel features:

- Overcurrent and overvoltage protection
- CM filtering
- Dynamic preloads (for zero-load needs)

Input protections

- Under-voltage Lockout
- Reverse polarity protection

TMTC:

Digital TMTC

- ON/OFF commands according to HV/LV-HPC
- ON/OFF Status telemetry according to BSM
- An ON/OFF logic based on redundant tel-ecommands and inner status (e.g. overcur-rent/overvoltage signals)

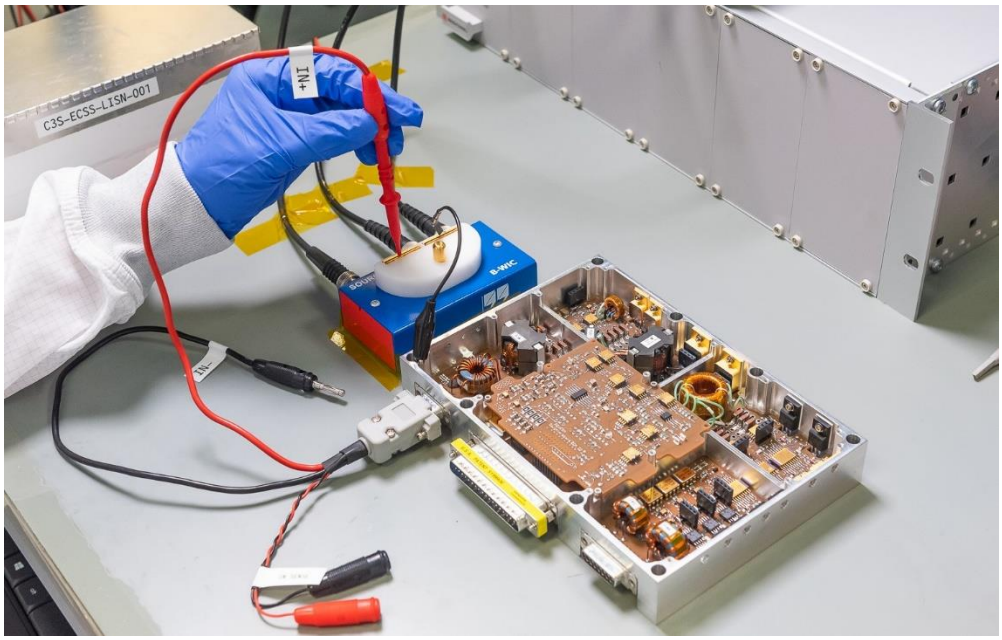
Analogue TMTC

- PT1000 thermistors for temperature te-lemetry
- Galvanically isolated current telemetry (4-20mA interface)

FM radiation level: TID: 50 krad

Temperature range: [-30°C, +60°C]

Figure 1: EQM of the Incentive Scheme PSU



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The EQM has already been manufactured, and measurements are ongoing - TRL 6 is not reached as of yet, but we expect it to be closed in May 2023 at the latest.

Table 1: Output parametes

	Implemented parameters		Customizable parameters	
Channel	**Nominal voltage**	**Maximum current**	**Minimum voltage**	**Maximum voltage**
Vmot_44Vp	44V	0.8A	3.3V	100V
Vmot_44Vn	-44V	0.8A	3.3V	100V
Vmot_15V	15V	0.15A	3.3V	100V

Note 1: Maximum possible output power on the converters is 200 W.

Note 2: Voltages on the output can't be higher than the minimal input voltage x2.

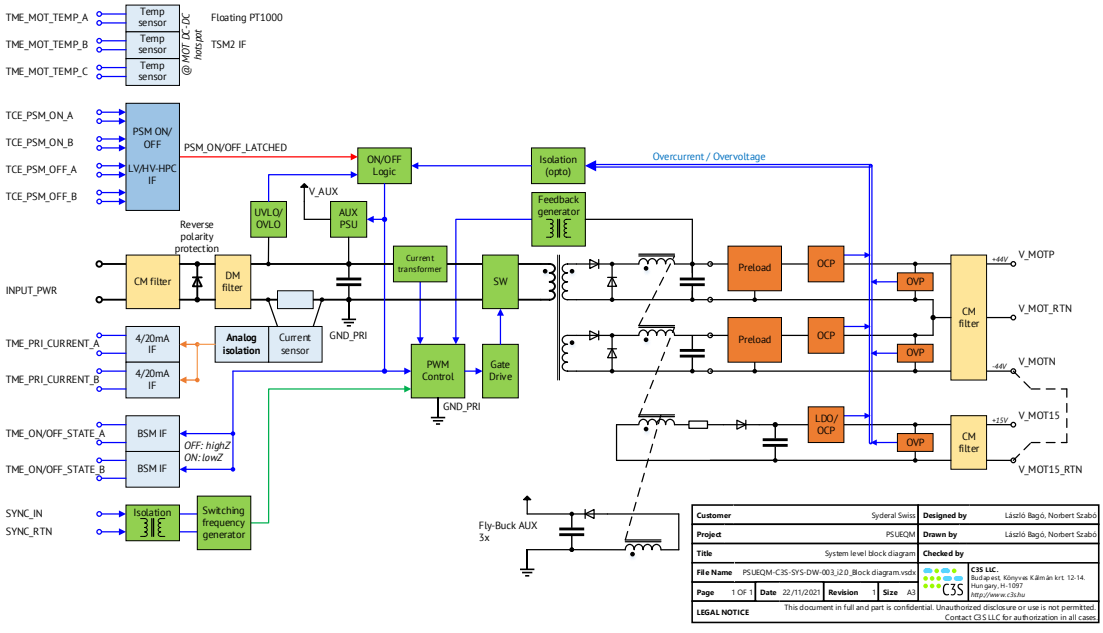
Note 3: The Vmot_15V channel (as it has a very small current) was implemented using a fly-buck architecture. Maximal power like this is limited to 5W, but having a channel like this is not mandatory.

Table 2: Input bus parameters

Versions	Implemented minimum voltage	Implemented nominal voltage	Implemented maximum voltage	Maximum viable voltage
28V bus version	22V	28V	38V	400V
50V bus version	32V	50V	52V	400V

Note 1: An input voltage range should have a smaller range (Maximal voltage/Minimal voltage) than a factor of 2 for an efficient design.

Figure 2: Block diagram of the Incentive Scheme DCDC



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